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(54) Lead-on-chip inner lead bonding lead frame, bonding method and apparatus.

(57) A multi-level lead frame configuration (114) for an integrated circuit chip (116) comprises a main lead frame (115) having a plurality of lead frame bond fingers (122 and 124) that directly connect to a plurality of bond pads (126) on the integrated circuit chip (116). Associated with the main lead frame (115) is a bus bar lead frame (128 and 130) having a plurality of bus bar lead fingers (118 and 120) that directly connect to a second plurality of inner bond pads (126) on the integrated circuit chip (116). The bus bar bond fingers (118 and 120) associate with the main lead frame (115) and main lead frame bond fingers (122 and 124) to permit a lead-on-chip configuration of the main lead frame and the bus bar lead frame.

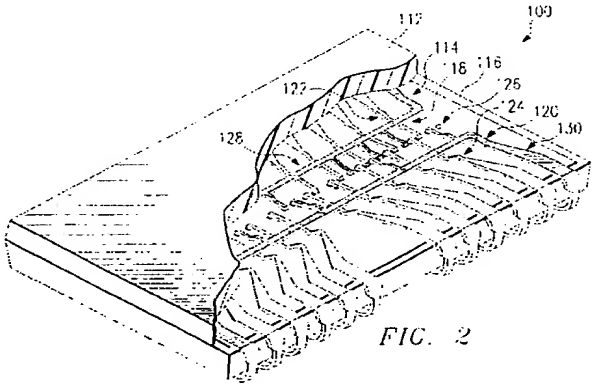

FIG. 2

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TECHNICAL FIELD OF THE INVENTION

The present invention generally relates to packaging of electronic devices and more particularly relates to a lead-on-chip inner lead bonding method and apparatus that permits direct inner lead bonding of a lead frame to bonding pads of an integrated circuit chip.

BACKGROUND OF THE INVENTION

Lead-on-chip semiconductor packaging structures use a lead frame that extends over and is adhesively joined to the surface of the integrated circuit chip. The lead frame has numerous bond fingers to carry signals between the chip and external circuitry. The bond fingers electrically connect via numerous bonding wires to bond pads typically located in a center row of the chip's top surface. In most lead frame configurations, the bond fingers appear on two sides of the bond pads. In lead-on-chip packages, a double-sided adhesive tape is used to attach the bond fingers to the chip and provide insulation between the chip and bond fingers. An advantage of this type of configuration is that power buses for the circuitry of the integrated circuit chip may be located external to the chip. In other words, the power buses may be part of the lead frame design. One merit of this packaging concept is that the power buses of the circuitry can be located external to the chip as part of the lead frame design. This reduces the chip size and improves the plastic-to-silicon ratio in the lead-on-chip package. The buses run alongside the bond pads. Connections between the bond pads and the bond fingers are, therefore, made by routing the bonding wires around the buses.

More modern lead-on-chip configurations avoid the use of bonding wires and, instead, connect bond fingers from a lead frame directly to the bond pads on the chip. Techniques that use these configurations are called inner lead bonding or ILB techniques. Power buses that run alongside the bond pads and must be routed around limit the ability to employ ILB techniques. With the power bus obstructing access to the bonding pads of the integrated circuit, it is not possible to easily access the bond pads with ILB lead frames.

There is a need, therefore, for a method to employ inner lead bonding techniques on an integrated circuit chip that uses lead-on-chip packaging.

There is a need for an apparatus that functions as a power bus for an integrated circuit chip and that permits an inner leading bonding adaptation to a lead-on-chip lead frame configuration.

SUMMARY OF THE INVENTION

The present invention, accordingly, provides a lead-on-chip lead frame configuration for use with inner lead bonding integrated circuit packaging techniques and that overcomes or reduces disadvantages and limitations associated with prior lead frame design and lead-on-chip circuitry connection methods.

One aspect of the invention is a multi-level lead frame configuration for an integrated circuit chip that has a main lead frame with a plurality of lead frame bond fingers. In the present invention, the bond fingers directly connect to a first plurality of inner bond pads on the integrated circuit chip. Additionally, the invention uses at least one bus bar that has a plurality of bus bar bond fingers to directly connect to a second plurality of inner bond pads on the integrated circuit chip. The bus bar bond fingers associate with the lead frame bond fingers to permit a lead-on-chip configuration of the main lead frame and the bus bar.

A technical advantage of the present invention is that it uses a double-level or multi-level lead frame configuration to facilitate direct inner lead bonding of the bond fingers with the bond pads using a half-etched lead frame for a single row of bond pads in the center of the chip. This permits inner lead bonding for both the power bus and the main lead frame.

Another technical advantage of the present invention is that it avoids the need for bonding wire by using inner lead bonding techniques, while at the same time employing lead-on-chip center bond connecting methods.

Another technical advantage of the present invention is that the bus bar pieces are downset at a different location from the main lead frame so that the bus bar may be stacked on the main lead frame. Additionally, in the present invention the bus bar bond fingers and the lead frame bond finger are on a different plane from that of the bus bar and main lead frame closer to the chip surface plane. This double-level configuration permits connecting the bus bar and the main lead frame with various different attaching methods, including an external lead bonding method and an insulating double-side adhesive tape.

BRIEF DESCRIPTION OF THE DRAWINGS

The invention and its modes of use and advantages are best understood by reference to the following description of illustrative embodiments when read in conjunction with the accompanying drawings, wherein:

FIGURE 1 illustrates a conventional lead frame configuration for lead-on-chip packaging;

FIGURE 2 provides a cut-away isometric perspective of the lead frame and the bus bar configuration of the preferred embodiment;

FIGUREs 3a and 3b illustrate top and side views, respectively, of certain portions of the preferred embodiment of the present invention; and

FIGUREs 4a and 4b show top and side views, re-

spectively, of an alternative embodiment of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

The preferred embodiment of the present invention is best understood by referring to the FIGUREs wherein like numerals are used for like and corresponding parts of the various drawings.

FIGURE 1 is an exploded view of the conventional lead-on-chip configuration for integrated circuit chip package 10. Within package 10 and under protective layer 12, lead frame 14 provides connections to circuitry within integrated circuit chip 16. Lead frame 14 includes two bus bars 18 and 20 and two sets of bond fingers 22 and 24. Connections of bus bars 18 and 20 and bond fingers 22 and 24 to bond pads 26 are made by bond wires 28.Several new techniques now permit inner lead bonding (ILB) of a lead frame to provide for direct connection of lead frame bond fingers to bond pads. The configuration of FIGURE 1, however, prohibits this. This is because bus bars 18 and 20 on lead frame 14 form a barrier to bond pads 26.

FIGURE 2 illustrates the preferred embodiment of the present invention and shows how the limitations of the prior art are overcome. In particular, integrated circuit chip package 100 of FIGURE 2 includes dual-level lead frame configuration 114 that is formed around or folded over the sides of integrated circuit chip 116. Dual-level lead frame 114 includes ILB bus bar bond fingers 118 and 120, as well as ILB lead frame fingers 122 and 124. Bus bar bond fingers 118 and 120 and lead frame bond fingers 122 and 124 connect directly to bond pads 126. This avoids the need to use bonding wires and provides to integrated circuit chip package 100 all of the benefits associated with inner lead bonding techniques. Bus bar bond fingers 118 and 120 are integral to bus bar pieces 128 and 130. Bus bar pieces 128 and 130 are separate bars that are attached to both main lead frame fingers 122 and associated support structure 132 and 134 of lead frame 114.

FIGUREs 3a and 3b illustrate the construction of the preferred embodiment of the present invention. In particular, FIGURE 3a shows a top view of the double-level lead frame 114 of the preferred embodiment in a fabrication pattern that may be employed using established fabrication techniques. Double-level lead frame 114 is formed from essentially three pieces. They include main lead frame 115, bus bar frame 128 and bus bar frame 130. Main lead frame bond fingers 122 and 124 protrude to centerline 136 for contacting bond pads 126 upon being placed over an integrated circuit chip. For power bus connects, bus bar frames 128 and 130 provide bus bar bond fingers 118 and 120, respectively, that also extend to centerline 136 for connecting to appropriate ones of bond pads 126.

In order to stack bus bar ILB frame 128 over main lead frame 115, it is necessary to have the two types of lead frame structures formed in a double-level configuration. FIGURE 3b illustrates a side perspective view of the relationship between bus bar lead frame 128 and main lead frame 122. In particular, bus bar lead frame 128 has an upper level portion 138 that goes to a lower level portion 140 by way of connecting piece 142. Also, main lead frame 115 includes upper portion 144 that connects to lower portion 146 by way of connecting piece 148. Note that at points 150 and 152, bus bar lead frame 128 joins main lead frame 115. This may be accomplished by any one of numerous well-established external lead bonding methods.

FIGUREs 4a and 4b illustrate, respectively, top and side views of an alternative embodiment of the present invention. In particular, bus bar ILB lead frames 128' and 130' are stacked over main lead frame 115 using an adhesive tape. FIGURE 4 shows adhesive tape 154 that is placed between top portion 138 of bus bar ILB 128' and bottom portion 146 of main lead frame 115. Tape 154 is a double-sided adhesive tape that is typically used in semiconductor chip manufacturing processes (e.g., comprising a Kapton or polyimide material). In the configuration of 4a and 4b, bus bar lead frame 128' and 130' may extend to external circuitry from main lead frame 115 by connecting and overlying structures 132 and 134 of main lead frame 115.

In summary, there has been shown a double-level lead frame configuration that permits direct inner lead bonding or ILB in a lead-on-chip center bond integrated circuit package and that includes a main lead frame having a plurality of lead frame bond fingers that directly connect to a first plurality of inner bond pads on an integrated chip together with at least one bus bar lead frame that has a plurality of bus bar bond fingers to directly connect to a second plurality of inner bond pads on the integrated circuit chip so that the main lead frame and the bus bar bond fingers permit a lead-on-chip configuration of the main lead frame and the bus bar lead frame.

Although the invention has been described with reference to the above-specified embodiments, this description is not meant to be construed in a limiting sense. Various modifications of the disclosed embodiment, as well as alternative embodiments of the invention will become apparent to persons skilled in the art upon reference to the above description. It is, therefore, contemplated that the appended claims will cover such modifications that fall within the true scope of the invention.

Claims

1. A multi-level lead frame, comprising:
a main frame; and a lead frame connector

comprising,

a plurality of bond fingers each having a first end for direct connection to bond pads of a semiconductor device and a second end connected to said main frame and connectable in use to external circuitry; and

at least one bus bar having a plurality of bus bar bond fingers for direct connection to bond pads of said semiconductor device and at least one bus bar bond finger connected to said main frame and connectable in use to external circuitry.

2. The lead frame of Claim 1, wherein said first ends of said plurality of bond fingers are on a first plane relative to said main frame and said at least one bus bar is on a second plane relative to said main frame.

3. The lead frame of Claim 2, wherein said second plane is on the same plane as said main frame.

4. The lead frame of Claim 2 or Claim 3, including an insulator between said at least one bus bar and said bond fingers on said first plane.

5. The lead frame of any preceding Claim, wherein said at least one bus bar traverses said plurality of bond fingers.

6. The lead frame of any preceding Claim, wherein said second ends of said plurality of bond fingers and said at least one bus bar bond finger are formed around or folded over side surfaces of said semiconductor device.

7. A lead frame assembly comprising a plurality of lead frames according to any of Claims 1 to 6, connected one to another.

8. The assembly of Claim 7, wherein the lead frames are connected one to another in a linear arrangement.

9. A device, comprising lead frame connectors according to any of claims 1 to 6, and a semiconductor device having bond pads located in at least one center row of a surface of said semiconductor device.

10. The device of Claim 9, wherein said first plane is between said surface of said semiconductor device having bond pads and said second plane.

11. A method, comprising:

providing a main frame and providing lead frame connectors comprising providing a plurality of bond fingers each having a first end connectable to the bond pads of a semiconductor device and a second end connectable to the main frame or in use in external circuitry; and

providing at least one bus bar having a plurality of bus bar bond fingers connectable to the second bond pads and of said semiconductor device at least one bus bar bond finger for connection to external circuitry.

12. The method of Claim 11, further comprising providing said first ends of said plurality of bond fingers on a first plane relative to said surface of said semiconductor device having bond pads and providing said at least one bus bar on a second plane relative to said surface of said semiconductor device.

13. The method of Claim 11 or Claim 12, further comprising providing said second ends of said plurality of bond fingers and said at least one bus bar bond finger for connection to external circuitry formed around or folded over side surfaces of said semiconductor device.

14. The method of Claim 12 or Claim 13, further comprising including an insulator between said at least one bus bar and said bond fingers on said first plane.

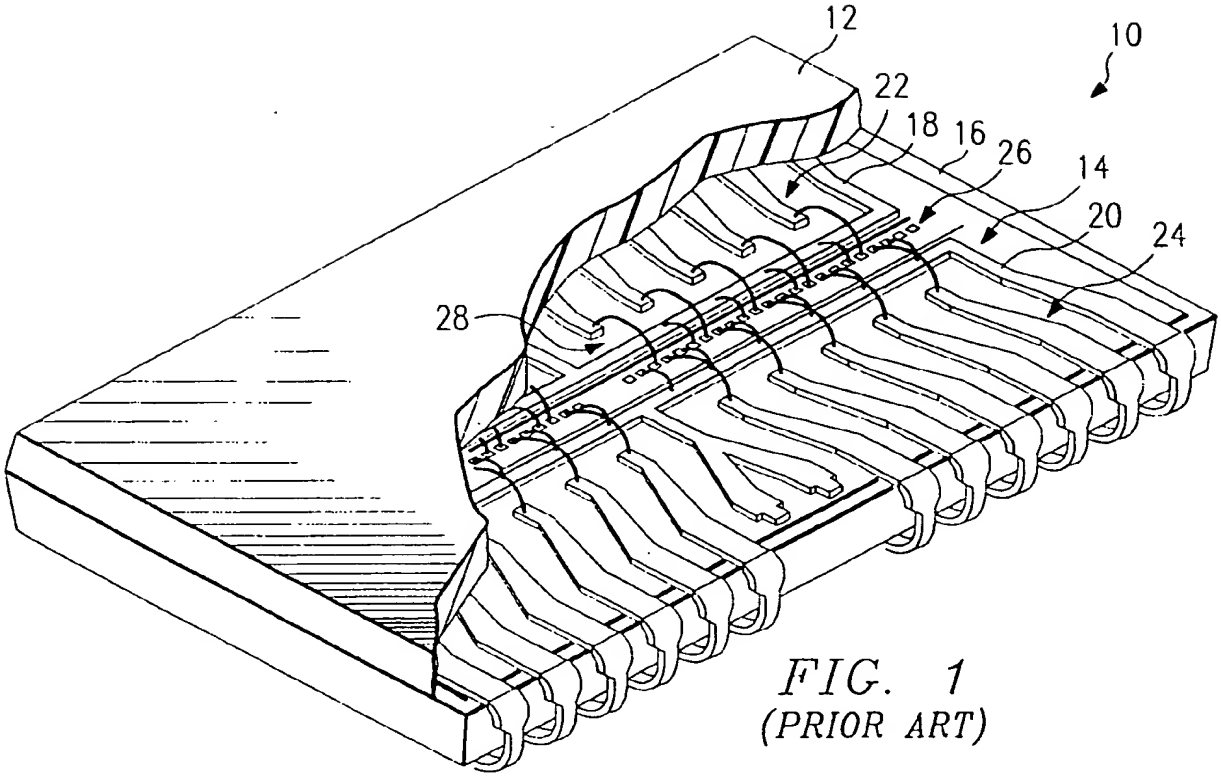


FIG. 1
(PRIOR ART)

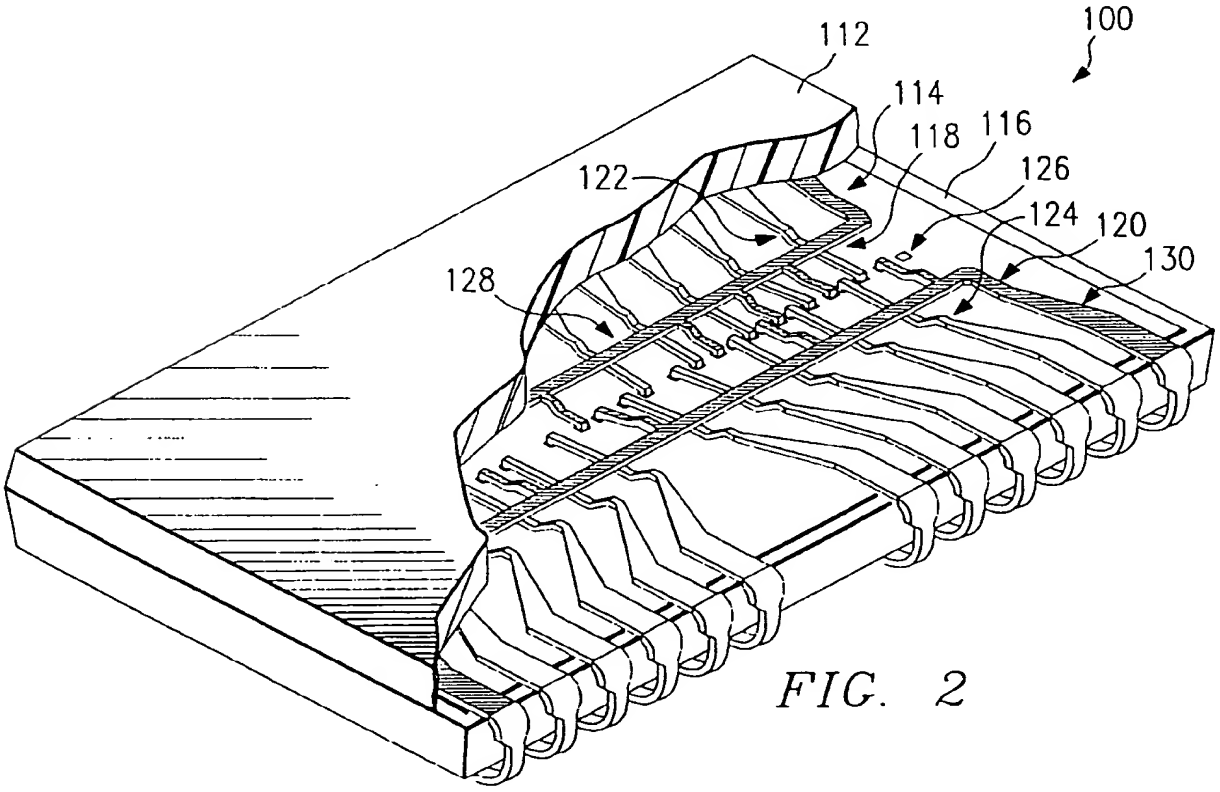
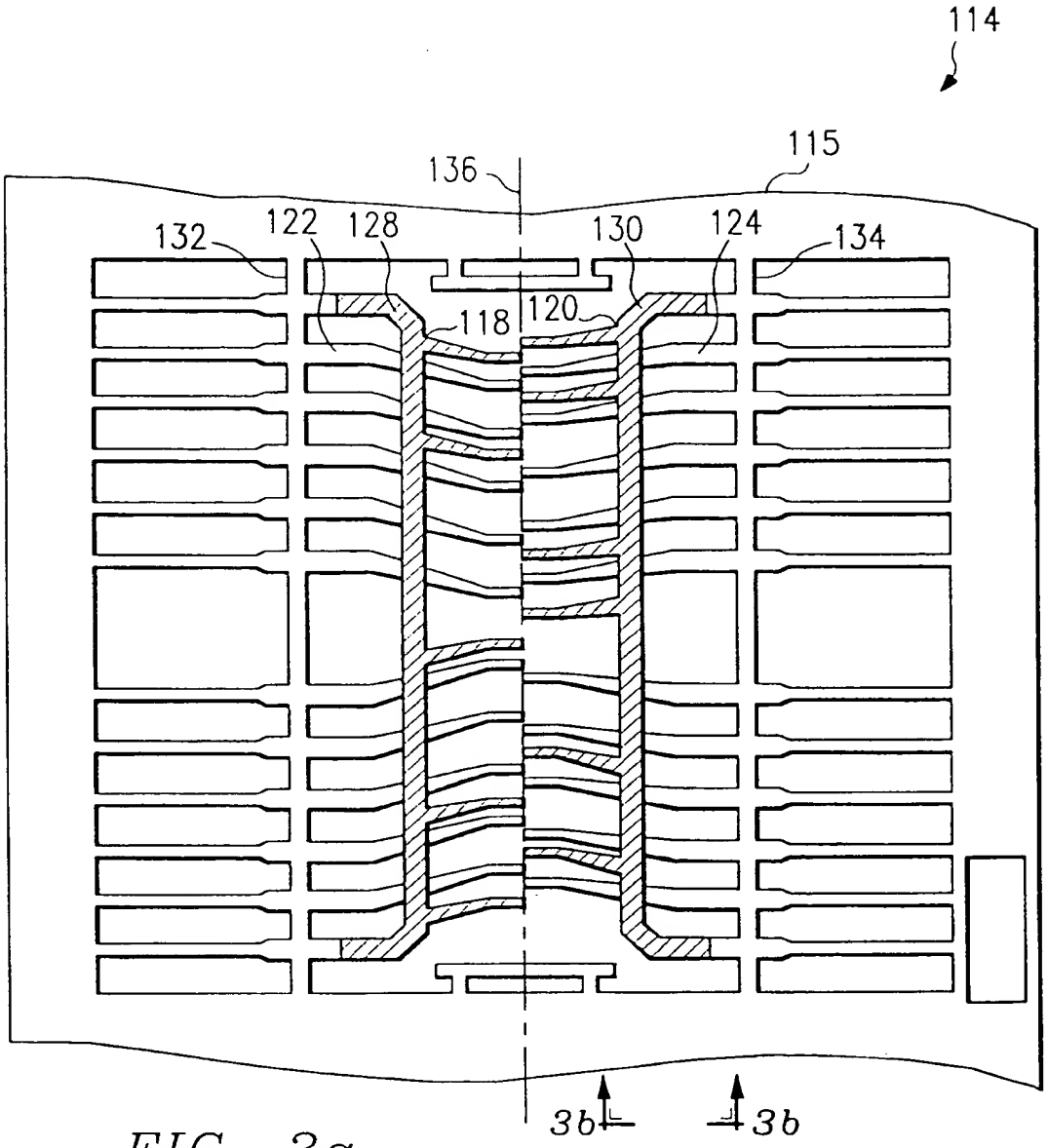


FIG. 2


114
115
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132
122
128
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118
120
3b
3b

FIG. 3a

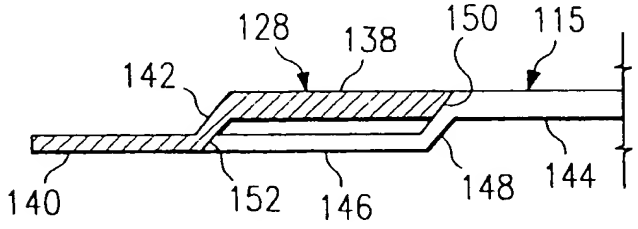
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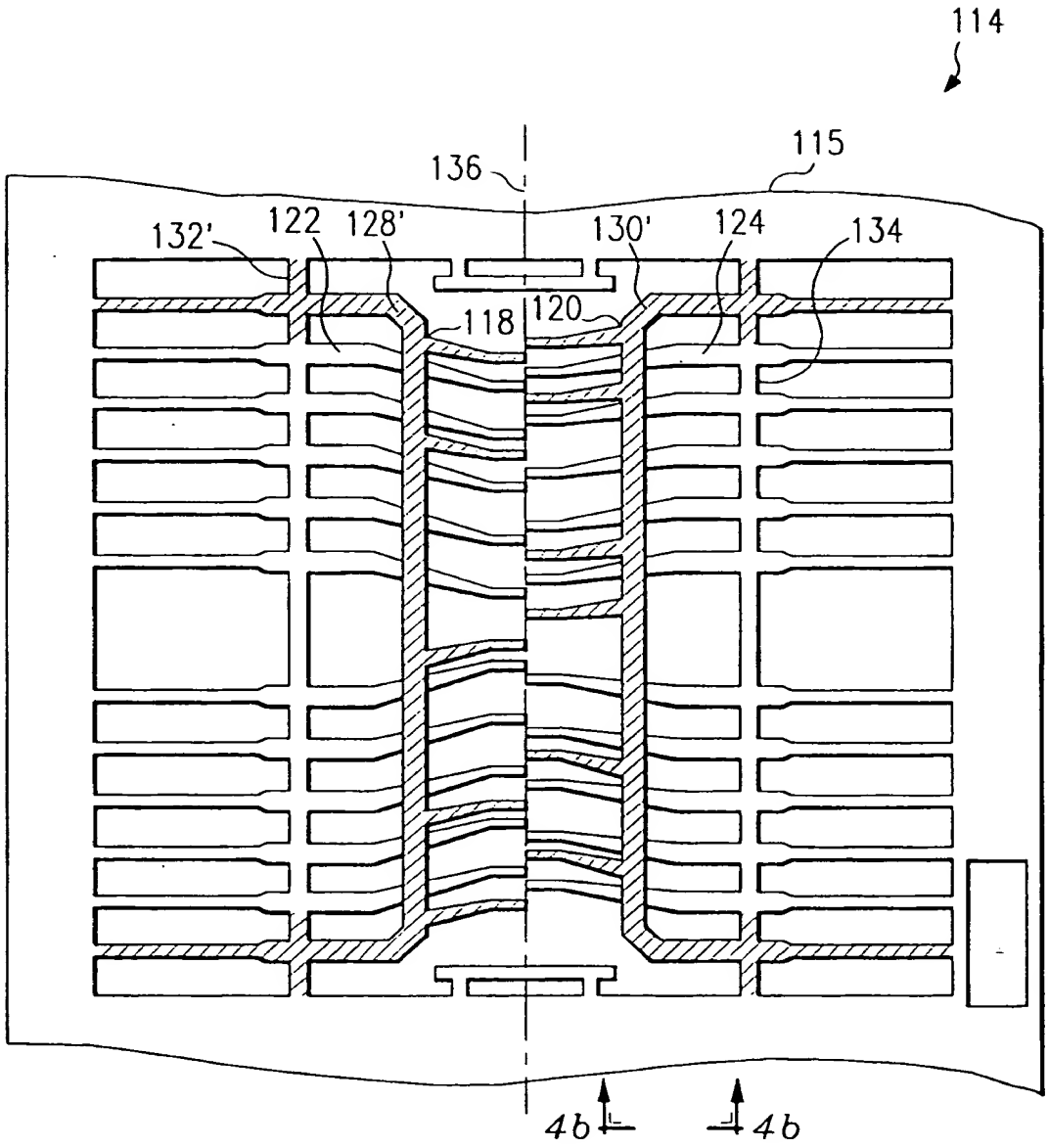
FIG. 3b


114
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4b

FIG. 4a

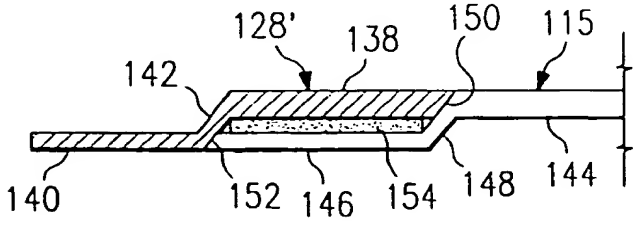
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FIG. 4b

European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 93 30 7781

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.5)
Y	PATENT ABSTRACTS OF JAPAN vol. 6, no. 211 (E-137)(1089) 23 October 1982 & JP-A-57 114 261 (HITACHI SEISAKUSHO K.K.) * abstract *	1-3,6,9, 11-13	H01L23/495 H01L23/50
Y	EP-A-0 478 250 (TEXAS INSTRUMENTS INCORPORATED) * the whole document *	1-3,6,9, 11-13	
P,X	DE-A-42 30 039 (MITSUBISHI DENKI K.K.) * the whole document *	1-14	
P,A	US-A-5 206 536 (LIM) * the whole document *	1-14	
P,A	DE-A-42 15 471 (GOLDSTAR ELECTRON CO., LTD.) * figures *	1-14	

TECHNICAL FIELDS SEARCHED (Int.Cl.5)

H01L

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	28 December 1993	Prohaska, G

CATEGORY OF CITED DOCUMENTS

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